Amendments to the Claims:

This listing of claims will replace all prior version, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A structure for flash memory cells ~~with improved endurance characteristics~~, comprising:

a semiconductor region within a substrate;

first ~~type one~~ isolation regions, separating cells, and second ~~type two~~ isolation regions, separating programming bit line channel regions of a cell from reading bit line channel regions of a cell, delineating active regions contained within said semiconductor region;

a conductive floating gate, for each cell, having a first floating gate portion disposed over the active region in the programming bit line channel region of a cell and a second floating gate portion disposed over the active region in the reading bit line channel region of the cell, both said first and said second floating gate portions being separated from said active regions by a floating gate insulator layer disposed over said active regions, and a third floating gate portion passing over said second ~~type two~~ isolation region to connect said first floating gate portion and second floating gate portion, wherein width of said first floating gate portion is narrower than width of said second floating gate portion;

a conductive control gate separated from said floating gate by an intergate insulator layer and from said semiconductor region by a control gate insulator layer and having a first control gate portion entirely disposed over said first floating gate portion, where said first floating gate portion completely covers the space between a first source region and a first drain region, having a second control gate portion disposed over said second floating gate portion, where said second floating gate portion does not extend all the way from a second source region to second drain region, said second control gate region completing the covering

of the space between said second source region and said second drain region and having a third control gate portion disposed over said third floating gate portion and connecting said first control gate portion and second control gate portion;

a covering insulator layer with a programming bit line channel contact line disposed over said covering insulator layer and connecting to said first drain region through said covering insulator layer and a reading bit line channel contact line disposed over said covering insulator layer and connecting to said second drain region through said covering insulator layer.

2. (Original) The structure of claim 1 wherein said semiconductor region is a silicon region.

3. (Original) The structure of claim 1 wherein said substrate is a silicon substrate.

4. (Currently Amended) The structure of claim 1 wherein said first ~~type one~~ isolation region is a shallow trench isolation region.

5. (Currently Amended) The structure of claim 1 wherein said second ~~type two~~ isolation region is a shallow trench isolation region.

6. (Original) The structure of claim 1 wherein said floating gate is a polysilicon floating gate.

7. (Original) The structure of claim 1 wherein said floating gate insulator layer is an oxide layer.

8. (Original) The structure of claim 1 wherein said control gate is a polysilicon control gate.

9. (Original) The structure of claim 1 wherein said control gate insulator layer is an oxide layer.

10. (Original) The structure of claim 1 wherein said intergate insulator layer is an oxide layer grown over said floating gate.

11. (Original) The structure of claim 1 wherein said first source region is formed by ion implantation.

12. (Original) The structure of claim 1 wherein said first drain region is formed by ion implantation.

13. (Original) The structure of claim 1 wherein said second source region is formed by ion implantation.

14. (Original) The structure of claim 1 wherein said second drain region is formed by ion implantation.

15. (Original) The structure of claim 1 wherein said covering insulator layer is an oxide layer, a nitride layer or an oxynitride layer or a composite layer formed from two or more of the set: oxide layer, nitride layer, oxynitride layer.

16. (Original) The structure of claim 1 wherein said programming bit line channel contact line is a polysilicon line.

17. (Original) The structure of claim 1 wherein said reading bit line channel contact line is a polysilicon line.

18. (Currently Amended) A method of forming flash memory cells ~~with improved endurance characteristics~~, comprising:

providing a semiconductor region within a substrate;

forming first ~~type one~~ isolation regions, separating cells, and forming second ~~type two~~ isolation regions, separating programming bit line channel regions of a cell from reading bit line channel regions of a cell, first ~~type one~~ isolation regions and second ~~type two~~ isolation regions delineating active regions contained within said semiconductor region;

forming a conductive floating gate, in each cell, where a first floating gate portion is disposed over the active region in the programming bit line channel region of a cell and a second floating gate portion is disposed over the active region in the reading bit line channel region of the cell, both said first and said second floating gate portions being separated from said active regions by a floating gate insulator layer formed over said active regions, and a third floating gate portion passes over said second ~~type two~~ isolation region to connect said first floating gate portion and second floating gate portion, wherein width of said first floating gate portion is narrower than width of said second floating gate portion;

forming a conductive control gate separated from said floating gate by an intergate insulator layer formed over said floating gate and from said semiconductor region by a control gate insulator layer formed over the active region and where a first control gate portion is entirely disposed over said first floating gate portion, where said first floating gate portion is formed to completely cover the space between a first source region and a first drain region, and a second control gate portion is disposed over said second floating gate portion, where said second floating gate portion is formed so as not to extend all the way from a second

source region to second drain region, said second control gate region being formed to complete the covering of the space between said second source region and said second drain region and with a third control gate portion formed to be disposed over said third floating gate portion and connecting said first control gate portion and second control gate portion;

forming a covering insulator layer and forming a programming bit line channel contact line disposed over said covering insulator layer and connecting to said first drain region through said covering insulator layer and forming a reading bit line channel contact line disposed over said covering insulator layer and connecting to said second drain region through said covering insulator layer.

19. (Currently amended) The ~~structure~~ method of claim 18 wherein said semiconductor region is a silicon region.

20. (Currently amended) The ~~structure~~ method of claim 18 wherein said substrate is a silicon substrate.

21. (Currently amended) The ~~structure~~ method of claim 18 wherein said first ~~type one~~ isolation region is a shallow trench isolation region.

22. (Currently amended) The ~~structure~~ method of claim 18 wherein said second ~~type two~~ isolation region is a shallow trench isolation region.

23. (Currently amended) The ~~structure~~ method of claim 18 wherein said floating gate is a polysilicon floating gate.

24. (Currently amended) The ~~structure~~ method of claim 18 wherein said floating gate insulator layer is an oxide layer.

25. (Currently amended) The ~~structure~~ method of claim 18 wherein said control gate is a polysilicon control gate.

26. (Currently amended) The ~~structure~~ method of claim 18 wherein said control gate insulator layer is an oxide layer.

27. (Currently amended) The ~~structure~~ method of claim 18 wherein said intergate insulator layer is an oxide layer grown over said floating gate.

28. (Currently amended) The ~~structure~~ method of claim 18 wherein said first source region is formed by ion implantation.

29. (Currently amended) The ~~structure~~ method of claim 18 wherein said first drain region is formed by ion implantation.

30. (Currently amended) The ~~structure~~ method of claim 18 wherein said second source region is formed by ion implantation.

31. (Currently amended) The ~~structure~~ method of claim 18 wherein said second drain region is formed by ion implantation.

32. (Currently amended) The ~~structure~~ method of claim 18 wherein said covering insulator layer is an oxide layer, a nitride layer or an oxynitride layer or a composite layer formed from two or more of the set: oxide layer, nitride layer, oxynitride layer.

33. (Currently amended) The ~~structure~~ method of claim 18 wherein said programming bit line channel contact line is a polysilicon line.

34. (Currently amended) The ~~structure~~ method of claim 18 wherein said reading bit line channel contact line is a polysilicon line.

35. (Currently Amended) A structure for flash memory cells with improved endurance characteristics, comprising:

[[A]] a semiconductor region within a substrate;

first ~~type one~~ isolation regions, separating cells, and second ~~type two~~ isolation regions, separating programming bit line channel regions of a cell from reading bit line channel regions of a cell, delineating active regions contained within said semiconductor region;

a conductive floating gate, for each cell, having a first floating gate portion disposed over the active region a conductive floating gate, for each cell, having a first floating gate portion disposed over the active region in the programming bit line channel region of a cell and a second floating gate portion disposed over the active region in the reading bit line channel region of the cell, both said first and said second floating gate portions being separated from said active regions by a floating gate insulator layer disposed over said active regions, and a third floating gate portion passing over said second ~~type two~~ isolation region to connect

said first floating gate portion and second floating gate portion, wherein width of said first floating gate portion is narrower than width of said second floating gate portion;

a conductive control gate separated from said floating gate by an intergate insulator layer and from said semiconductor region by a control gate insulator layer and having a first control gate portion entirely disposed over said first floating gate portion, where said first floating gate portion is disposed between a first source region and a first drain region and is wider than said second floating gate portion, having a second control gate portion disposed over said second floating gate portion, where said second floating gate portion does not extend all the way from a second source region to second drain region, said second control gate portion, that is wider than said first control gate portion, also covers a space between said second source region and said second drain region and having a third control gate portion disposed over said third floating gate portion and connecting said first control gate portion and second control gate portion;

a covering insulator layer with a programming bit line channel contact line disposed over said covering insulator layer and connecting to said first drain region through said covering insulator layer and a reading bit line channel contact line disposed over said covering insulator layer and connecting to said second drain region through said covering insulator layer.

36. (Original) The structure of claim 35 wherein said semiconductor region is a silicon region.

37. (Original) The structure of claim 35 wherein said substrate is a silicon substrate.

38. (Original) The structure of claim 35 wherein said first ~~type one~~ isolation region is a shallow trench isolation region.

39. (Original) The structure of claim 35 wherein said second ~~type two~~ isolation region is a shallow trench isolation region.

40. (Original) The structure of claim 35 wherein said floating gate is a polysilicon floating gate.

41. (Original) The structure of claim 35 wherein said floating gate insulator layer is an oxide layer.

42. (Original) The structure of claim 35 wherein said control gate is a polysilicon control gate.

43. (Original) The structure of claim 35 wherein said control gate insulator layer is an oxide layer.

44. (Original) The structure of claim 35 wherein said intergate insulator layer is an oxide layer grown over said floating gate.

45. (Original) The structure of claim 35 wherein said first source region is formed by ion implantation.

46. (Original) The structure of claim 35 wherein said first drain region is formed by ion implantation.

47. (Original) The structure of claim 35 wherein said second source region is formed by ion implantation.

48. (Original) The structure of claim 35 wherein said second drain region is formed by ion implantation.

49. (Original) The structure of claim 35 wherein said covering insulator layer is an oxide layer, a nitride layer or an oxynitride layer or a composite layer formed from two or more of the set: oxide layer, nitride layer, oxynitride layer.

50. (Original) The structure of claim 35 wherein said programming bit line channel contact line is a polysilicon line.

51. (Original) The structure of claim 35 wherein said reading bit line channel contact line is a polysilicon line.

52. (New) a flash memory device, comprising:

a substrate,

a floating gate disposed overlying the substrate;

a control gate disposed overlying the floating gate;

a source region disposed in the substrate and adjacent to a first side of the floating gate;

a first drain region and a second drain region disposed in the substrate and adjacent to a second side of the floating gate; and

an isolation region disposed in the substrate and isolates the first and second drain region from each other, wherein width of a portion of the floating gate near the first drain region is smaller than another portion of the floating gate near the second drain region, and width of a portion of the control gate near the first drain region is larger than another portion of the control gate near the second drain region.